

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Visokay et al.	Docket No.:	TI-35227
Serial No.:	10/734,708	Art Unit:	2813
Filing Date:	12/11/2003	Examiner:	Thanhha S. Pham
Customer No.:	23494	Conf. No.:	2373

Title: Method for Fabricating Transistor Gate Structures and Gate Dielectrics Thereof

**TRANSMITTAL OF FORMAL DRAWINGS**

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

Attn: Official Draftsperson

Dear Sir:

Enclosed are five (5) sheets of formal drawings. These drawings are being submitted to replace drawings previously submitted on 12/11/2003.

Charge any necessary fee to Deposit Account No. 20-0668.

Respectfully submitted,

/Jacqueline J. Garner/  
Jacqueline J. Garner  
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